REMARKS

This Reply is considered fully responsive to the Final Office Action mailed November 2 2006. Claims 1-28 were pending in the application. Claims 14-28 are withdrawn from consideration. Claims 1-13 stand rejected. Claim 1 has been amended only to correct informalities. Claims 14-28 have been cancelled without prejudice or disclaimer. No new claims are added. In view of the following remarks, Applicants respectfully request reconsideration and allowance of the subject application.

Traversal of Election/Restriction

In the response to the non-final Office Action filed on August 9, 2006, Applicants elected claims 1-13 of the present application with traverse. Applicants acknowledge that the Office has considered Applicants' arguments, and the restriction requirement remains final. Applicants reserve the right to file a divisional, continuation, or continuation-in-part application covering the subject matter of the non-elected claims.

Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 1-13 under 35 U.S.C. § 103(a) as being purportedly unpatentable over U.S. Patent No. 6,653,331 to Masuda et al. ("Masuda") in view of U.S. Patent No. 6,680,219 to Reyes et al. ("Reyes"). All rejections are respectfully traversed.

Independent claim 1 recites, *inter alia*, at least two dice, each of said dice having at least one electrical connection disposed on a single surface, and said dice being electrically coupled with at least one connector between said electrical connections that are oriented in the same direction when said dice are stacked and offset; and a third die that is not stacked with said at least two dice, said third die being electrically connected directly to said at least one electrical connection of at least one of said at least two dice via a direct die-to-die connector.

The primary citation to Masuda relates to a semiconductor device and method of manufacturing the same. More specifically, Masuda discusses a stacking system in which the memory chips 1A are stacked in two layers and the upper memory chip 1A is stacked over the lower memory chip 1A while sliding the upper memory chip 1A in the X direction parallel to one side of the lower memory chip 1A and in the Y direction perpendicular thereto. Masuda at col. 5, lines 6-11, Figs. 4A, 4B). Further, Masuda discusses that the dice are electrically coupled with at least one connector between electrically common bonding pads oriented in the same

direction when the dice are stacked and offset as described above. Masuda at col. 5, lines 11-32, Fig. 4b.

At page 4 of the Office Action, the Office concedes that Masuda fails to teach or suggest "a third die that is not stacked with at least two dice, said third die being electrically connected directly to said at least one of said at least two dice via a direct die-to-die connector" and relies on the secondary citation to Reyes to teach this feature. Reyes relates to method and apparatus for die stacking. More specifically, Reyes discusses the stacking of dies which are then coupled to the substrate using die-to-substrate wire bonds and to each other with either die-to-die wire bonds or die-to-die wire bridges that span any lower wire bonds. Reyes at col. 2, lines 50-55. Absent from Reyes, however, is any teaching or suggestion that the third die, which is not stacked, is electrically connected to at least one electrical connection of at least one of said at least two stacked dice via a direct die-to-die connector.

Consequently, Applicants respectfully submit that the combination of Masuda and Reyes fails to disclose all of the features of independent claim 1. Accordingly, favorable reconsideration and withdrawal of the rejection of the independent claim 1 under 35 U.S.C. § 103. Allowance of claim 1 is respectfully requested.

Claims 2-13 depend from claim 1, which is believed to be allowable. Accordingly, claims 2-13 are believed to be allowable for at least the same reasons as claim 1. As such, allowance of claims 2-13 is respectfully requested.

Further, Applicants respectfully submit that neither Masuda nor Reyes expressly or impliedly suggest the asserted combination, as recited in independent claim 1. Indeed, Applicants note no such contention in the Office Action. Thus, as part its initial burden to establish a *prima facie* case of obviousness, the Office "must present a convincing line of reasoning as to why the artisan would have found the claimed invention to be obvious in light of the teachings of the references. MPEP §2142, citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

Section 2142 of the Manual of Patent Examining Procedure ("MPEP") explains that a *prima facie* case of obviousness requires that there be some suggestion or motivation, either in the references themselves of in the knowledge of one of ordinary skill in the art, to modify combine reference teachings. It is for this reason that the mere fact that a combination can be

made is legally insufficient to support an obviousness rejection. MPEP §2143.01. And, the Office bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the Office does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of nonobviousness. MPEP §2142. Applicants respectfully submit that such is the case in the present application.

The Office Action provides a single line of reasoning for the alleged motivation to make the asserted combination. Specifically, at page 4 of the Office Action, it is asserted that one of ordinary skill in the art would have been motivated to modify Masuda in view of Reyes "to improve the circuit density of the Masuda stacked IC package more efficiently and more cost effective[ly] as taught by Reyes in column 1 lines 53-55." Applicants note that Reyes at column 1, lines 53-55 merely states that "There is a resulting need for a more efficient and less expensive method for increasing the circuit density of an IC-package by die stacking." Thus, it is asserted that one of ordinary skill in the art would have been motivated to modify Masuda's teaching of stacking dies in view of Reyes's teaching of electrically connecting stacked dice to increase the circuit density of an IC-package by die stacking.

This line of reasoning, however, does not meet the MPEP's required standard of "convincing" because Masuda achieves this result without the asserted modification *See, e.g.*, Masuda, Abstract. Stated another way, the capability to stack dice is already provided by Masuda alone. Further, Masuda teaches that advantages of this die stacking method include "a size and thickness reduction of a semiconductor device having a plurality of semiconductor chips stacked on one another..." and "reducing the manufacturing cost of a semiconductor device having a plurality of semiconductor chips stacked on one another...." Masuda at col. 2, lines 6-13. Consequently, the Office Action fails to provide the required "convincing line of reasoning" required by the MPEP.

The absence of this convincing line of reasoning and any other suggestion for the asserted combination precludes a *prima facie* case of obviousness. For at least this reason, and those set forth above, the rejection of independent claim 1, and those claims depending directly or indirectly therefrom, under 35 U.S.C. § 103 are respectfully traversed. *See* MPEP §2142.

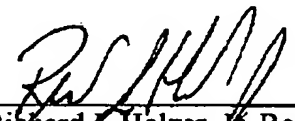
Conclusion

Applicants submit that this Reply clearly places the subject application in condition for allowance. The amendments herein were not earlier presented because Applicants believed that the prior Amendment placed the subject application in condition for allowance. Accordingly, entry of the instant Amendment as an earnest attempt to advance prosecution and reduce the number of issues is requested under 37 C.F.R. §1.116.

This Reply is believed to be responsive to all points raised in the Office Action. Accordingly, prompt allowance and passage of the application to issue are earnestly solicited. Should the Examiner have any remaining questions or concerns, he/she is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

1-3-07
Date



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